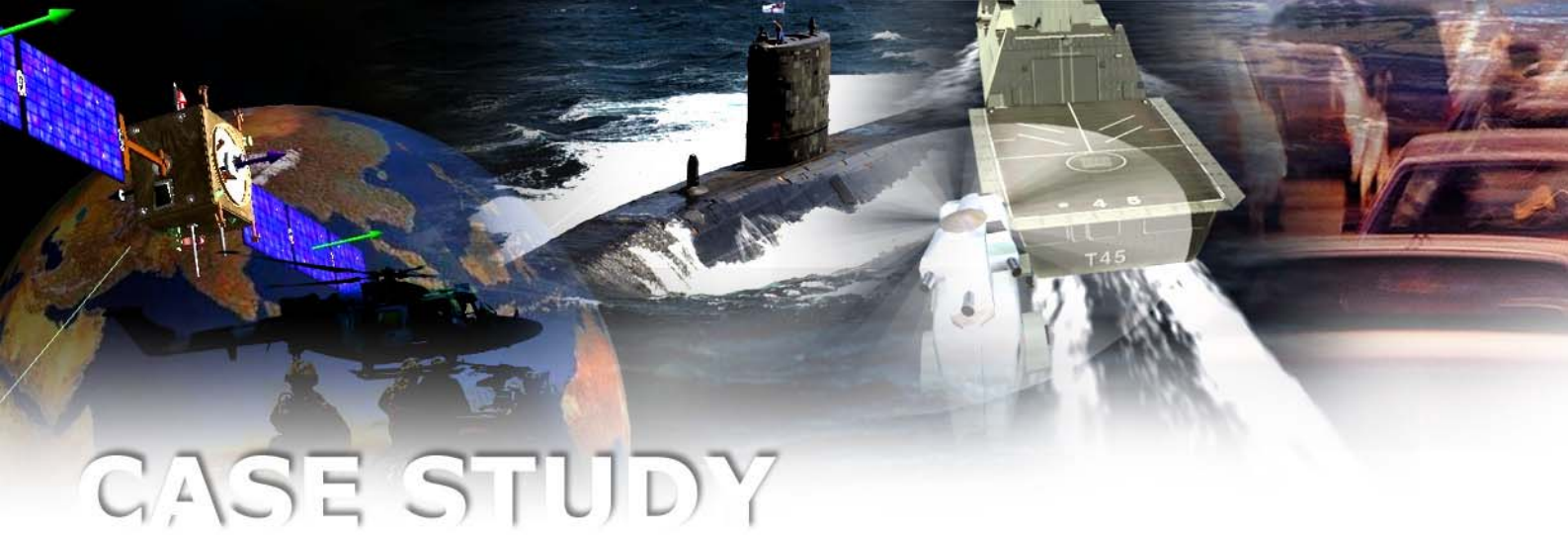

S-UMTS Processor Key Technologies Demonstrator

The Satellite – Universal Mobile Telecommunications System (S-UMTS) Processor Key Technologies Demonstration Hardware (SDH) has been designed, manufactured and tested by SEA. This equipment has a high level of design complexity (2,500 nets per card) yet the manufactured equipment was “right first time”, successfully achieving the full specification set by the customer without the need for any design updates. Technologies employed include Xilinx Virtex II Pro devices and comprehensive VHDL functional test code.

The SDH is a prototype for demonstrating a number of architectures and new technologies relevant to the next generation of mobile space missions. The top level system architecture is generic and modular but is supplemented by additional inter-FPGA data buses in the hardware design; this flexibility opens the possibility of spreading DSP functionality across the multiple FPGAs to implement different processing architectures.

The SDH consists of a 9U rack containing three custom designed cards (corresponding to the Feeder Module and two Mobile Modules) connected via a high-speed backplane. Each card contains 9 highly interconnected Xilinx Virtex-II Pro FPGA to provide a very high DSP performance capability. The use of FPGAs allows for complete reconfiguration of the hardware to use entirely different algorithms and to perform different or additional functions if desired. The FPGAs employed in the design are programmed using JTAG permitting different designs to be loaded for the analogue and digital test modes.

The ADCs and DACs are clocked at 112 MHz; the architecture permits acquired data to be de-interleaved by two, thus enabling the FPGAs to operate at a clock rate of 56 MHz. The ADCs and DACs are 12 bit devices and the overall performance of the system exceeded that of an ideal 9-bit converter. The processed band tests showed both the input and output passband flatness to be better than ±0.3 dB.

High speed serial links are implemented using multi-gigabit RocketIO transceivers which operate at 1.12 Gbps and use 8b/10b coding. In the system test environment the calculated data throughput (accounting for encoding overhead) is 35 Gbps across the complete backplane.